UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

AD

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
08/925,868	09/09/97	ISBARA	M	INPA:035

MM42/1101

WILLIAM W. KIDD
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES CA 90025

EXAMINER	
WELLS,K	

ART UNIT	PAPER NUMBER
2816	20

DATE MAILED: 11/01/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/925,868	ISBARA
Examiner	**Group Art Unit**
Kenneth B. Wells	2816

☒ Responsive to communication(s) filed on *10-12-99* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *three* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-20* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

Response to Amendment

1. The preliminary amendment filed on 10/12/99 has been entered in the case.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objections

3. Claim 8 is objected to because of the following informalities: on line 2, "a" is grammatically improper and should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over any one of Fox, Nelson and GB 1,2287,021.

As to claim 1, note that each of these references discloses an RC attenuator, which is essentially all that applicant is reciting in this claim. The differences are that applicant uses a continuously-on biased FET instead of the discrete resistor shown by each of the references. However, the replacement of a

discrete resistor with a continuously-on biased FET is notoriously well-known in the art (official notice is taken) and there is obvious motivation to make such a replacement, i.e., to save chip real estate, since discrete resistors take up more space than integrated FETs acting as resistance elements. The resistor recited in the claim also fails to distinguish patentably over these references because it is also old and well-known in the art to add such a series resistor between the gate bias voltage and the gate of the FET for the purpose of controlling the on level of the FET (and thereby controlling the resistance value of the FET), all of which are old and well-known concepts to those having ordinary skill in the art. The new limitations added to the claims, that the input and output signals are binary, does not define patentably over the applied prior art because, as applicant is well aware, the type of signals that are received and output by a certain device are not part of the device (i.e., they are not structural features of the invention) and thus are merely intended use limitations which cannot distinguish a claimed structure from a prior art structure which fully meets the claim under 35 USC 102 or 103. Moreover, note that the Nelson reference suggests using binary input and output signals (see Fig. 2 of that reference).

As to the remaining claims which recite the inverter 26 and pull-up FET 28, the limitations recited therein are also considered to be well-within the ordinary skill level and are thus obvious as well, for the reasons noted in the previous office actions.

Response to Arguments

5. Applicant's arguments filed on 6/18/99 have been fully considered but they are not persuasive.

The argument that applicant's claims are not anticipated because the prior art does not teach the claimed circuit used in the manner recited in the claims is incorrect because, as applicant is well aware, claims to circuitry must distinguish over the prior art under 102 and 103 by structure not function or how the circuit is used, see Ex parte Masham, 2 USPQ2d 1647 (1987) and In re Danley, 120 USPQ 528 (CCPA 1959). Note further MPEP 2114.

Applicant's next argument, that it would not have been obvious to substitute an FET for the resistor shown in each of the references because applicant has discovered a new use or function of the FET, is similarly without merit. As applicant is

well aware, it is only required that there be some motivation for making the substitution of art recognized equivalents, and applicant's particular reason for using the recited structure (and also any newly discovered property or characteristic that results therefrom) is irrelevant to the issue of obviousness.

The final argument, that the claimed invention recites binary inputs and outputs and thus defines over the applied prior art, is without merit for the reasons noted in paragraph four, supra.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth B. Wells whose telephone number is (703) 308-4809. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Kenneth B. Wells
Primary Examiner
Art Unit 2816

November 1, 1999